In the Claims:

Claims 1 - 18 (cancel)

Claim 19 (currently amended): A multilayer chip carrier, comprising:

a first layer of dielectric material having a plurality of signal pads formed thereon arranged in a pattern of signal pads related to signal pads within a footprint of at least one chip to be carried by said chip carrier, said plurality of signal pads including a first set of signal pads near the edge of said chip footprint with each pad of said first set of signal pads having a conductive line connected thereto extending beyond the edge of said chip footprint and a second set of signal pads with each pad of said second set of signal pads having a conductive line connected thereto extending to connect to respective signal pads of another set of signal pads positioned closer to the edge of said chip footprint with said another set of signal pads positioned closer to the edge of said chip footprint each having a conductive via connected thereto extending through said first layer of dielectric material to form a set of conductive vias in said first layer of dielectric material;

a second layer of dielectric material having a first set of signal pads formed thereon with respective ones of said first set of signal pads arranged to connect to respective ones of said set of conductive vias extending through said first layer of dielectric material and with each pad of said first set of signal pads having a conductive line connected thereto extending to connect to respective signal pads of a second set of signal pads on said second layer of dielectric material positioned closer to the edge of said chip footprint, each pad of said second set of signal pads having a conductive via connected thereto extending through said second layer of dielectric material to form a set of conductive vias in said second layer of dielectric material ; and

a third layer of dielectric material having a set of signal pads formed thereon with respective ones of said signal pads of said third layer of dielectric material arranged to connect ~~connected~~ to respective ones of said set of conductive vias extending through said second layer of dielectric material and with each pad of said set of pads on said third

layer of dielectric material having a conductive line connected thereto extending beyond the edge of said chip footprint.

Claim 20 (original): The multilayer chip carrier as set forth in Claim 19 including at least one chip having a pattern of electrical contacts corresponding to said pattern of signal pads electrically connected thereto.

Claim 21 (original): The multilayer chip carrier as set forth in Claim 20 wherein said chip carrier is electrically attached to a printed wiring board.

- Claims 22 - 30 (cancel)